DETERMINATION OF INTERFACE TRAP DENSITY IN MOS STRUCTURES USING ACOUSTOELECTRIC RESPONSE

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1. Introduction

It is well known that the interface traps at the Si–SiO_2 interface in the MOS (metal–oxide–semiconductor) structures play an important role in determining several characteristics of electronic devices ulitizing this structure. In recent years there has been an increased interest to find an accurate modelling and characterization of interface traps through the band gap, mostly using capacitance and conductance methods [1-4]. The measurement of acoustoelectric response (AER) of the MOS structure as a function of the gate bias voltage can be another method determining the energy distribution through the investigated MOS structure. The AER signal produced by MOS structure traversed by a longitudinal acoustic wave is namely extremely sensitive to any changes in the space charge distribution in the interface region of the MOS structure [5,6].

In this contribution, the first attempt to describe both the model for simulating the AER dependence on the external bias voltage ($U_{ac}^{0} - V_G$ curve) and the model describing the interface state distribution is presented.

2. Theoretical principles

The AER creation can be explained using the idea of an acoustic wave passing through the semiconductor structure with the space charge region characterized by a non-zero electric field, typical for p-n junctions, Schottky diods, MIS structures, heterostructures and so forth. The acoustic wave following the pressure modulation of charge density evoke the change of potential difference that manifests as AER signal. The AER depends on the electric field *E(x)* in the space charge region and the acoustic pressure *p(x,t)* and can be expressed by the general relation

$$U_{\mathrm{ac}}^{0}(t) = \int_{0}^{d} SE(x)\,p(x,t)\,dx\,, \tag{1}$$

where S expressed mainly elastic and dielelectric properties of investigated material and d is the width of active region. The AER produced by a semiconductor structure is then proportional, using the similarity with the case of electromechanical capacitance transducer, to the voltage and the relative change of capacitance induced by the acoustic wave. The relative change of capacitance can be directly replaced by the relative deformation for the case of thin planar structure ($d << \lambda$) [5].

The dependence of AER amplitude U_{ac}^{0} on the gate bias voltage V_G applied to the ideal MOS structure can be described by following equation:

$$U_{\mathrm{ac}}^{0}(V_G) = \frac{p_0}{K_{ox}} \frac{|Q(\varphi_s)|}{C_{ox}} + \frac{p_0}{K_s} |\varphi_s(V_G)| + U_{ac}^{0}(V_{FB}), \tag{2}$$

where p_0 is the acoustic pressure amplitude, Q is the density of the accumulated charge, K_{ox} and K_s are the oxide and the semiconductor elastic moduli, respectively, C_{ox} is the oxide capacitance, φ_s is the surface potential across the semicondictor and $U_{ac}^{0}(V_{FB})$ is the amplitude of AER at the flat band voltage V_{FB}. In general, gate bias voltage V_G relates to the surface potential φ_s as in the following equation:

$$V_G - V_{FB} = -\frac{Q(\varphi_s)}{C_{ox}} + \varphi_s . \tag{3}$$

To determine the energy distribution of interface traps it is necessary to know the dependence of surface potential on the gate bias voltage $\varphi_s = f(V_G)$ for the ideal MOS structure. This dependence can be obtained by numerical solution of the Eqn.3 using model [1], which suggests that the density of the accumulated charge in the Eqn.3 can be written for the n-MOS structure as:

$$Q(\varphi_s) = \pm \frac{2kT\varepsilon_0\varepsilon_s}{qL_D} \sqrt{\exp(\frac{q\varphi_s}{kT}) - \frac{q\varphi_s}{kT} - 1 + \frac{n_i}{N_D}(\exp(-\frac{q\varphi_s}{kT}) + \frac{q\varphi_s}{kT} - 1)}, \tag{4}$$

where k is Boltzman's constant, T is the thermodynamic temperature, ε_0 is the vacuum permitivity, ε_s is the dielectric constant of the semiconductor, q is the elementary charge, L_D is Debye's length, N_D is the concentration of the donors, n_i is the intrinsic concentration in the semiconductor, the sign plus is in the Eqn.4 for the depletion or inversion state and the sign minus for the accumulation state.

If we substitute on the right side of the Eqn.2 the dependences $\varphi_s = f(V_G)$ and $Q = f(\varphi_s)$ using considered model, we can obtain the dependence of the AER on the gate bias voltage for an ideal MOS structure. Now, when we know the both ideal and real voltage

dependence of the AER of the investigated MOS structure, we can determine the energy distribution of the interface traps. The traps causes the shift of the measured curve against the ideal curve by the value $\Delta V_G(\varphi_s)$ that is the function of the surface potential. Following the knowledge of the dependence $\Delta V_G(\varphi_s)$, the density of charge of interface traps can be calculated:

$$Q_{it}(\varphi_s) = C_{ox} \cdot \Delta V_G(\varphi_s). \tag{5}$$

This dependence is very important for determination of the energy distribution of interface traps. The energy distribution of the interface traps can be expressed using the equation [2]:

$$D_{it} = \frac{1}{q^2}\left|\frac{\partial Q_{it}(\varphi_s)}{\partial \varphi_s}\right|, \tag{6}$$

where D_{it} is the interface traps density.

The energy level E in the band gap of the semiconductor, corresponding to $D_{it}(E)$, can be calculate from the equation [7]:

$$E = E_v + \frac{E_g}{2} + q\varphi_s \pm kT \ln\left(\frac{N_{D,\,A}}{n_i}\right), \tag{7}$$

where E_v is the maximum of the semiconductor valence band, E_g is the semiconductor band gap, $N_{D,\,A}$ is the concentration of donors or acceptors, the plus sign is in the Eqn.7 for the n-MOS and the minus sign for the p-MOS structure.

3. Experimental

The block diagram of the experimental setup is illustrated in Fig. 1. The computer was used to trigger the system, to generate the gate bias voltage and moreover to record the

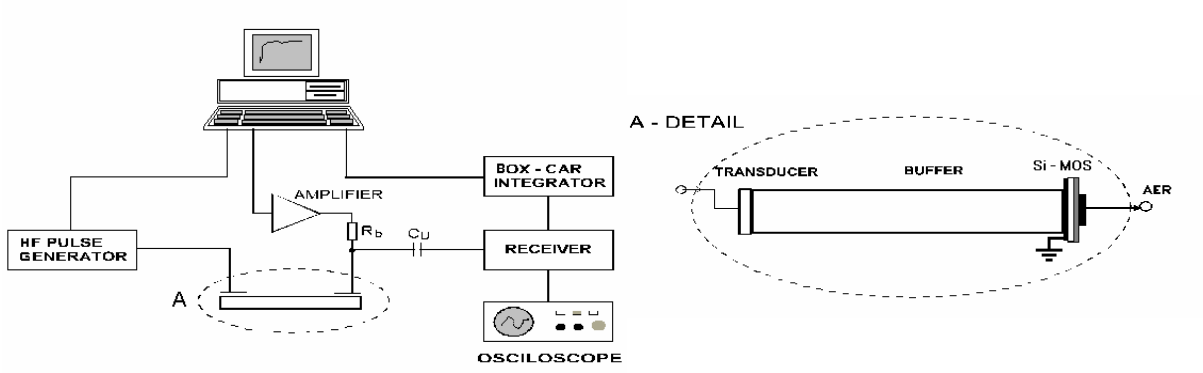

Fig.1: *Experimental arrangement for the $U_{ac}^{0}(V_G)$ dependence measurement.*

acoustoelectric response $U_{ac}^{0}(V_G)$. The longitudal acoustic waves of frequency 14,5 MHz were generated by $LiNbO_3$ transducer acoustically bonded to the quartz rod buffer. The MOS structure worked as a receiver transducer. The box-car integrator was used for the selection of the AER produced by the structure after detection in the receiver. Then the $U_{ac}^{0}(V_G)$ dependence was registered and stored by computer.

4. Results and discussion

We have investigated the energy distribution of the interface traps in two MOS structures (marked as Sample 1 and Sample 2) of the type Al–SiO_2–Si capacitor (see Tab.1).

marking	type	d_{ox} [nm]	$N_{D,A}$ [m^{-3}]	dopping element	V_{FB} [V]	T [K]	used acoustic pressure p_0 [GPa]
Sample 1	n - MOS	4	1.10^{21}	phosphorus	-0,6	300	67
Sample 2	p - MOS	80	5.10^{21}	boron	4,6	300	11,2

Tab.1: *The parameters of the investigated MOS structures.*

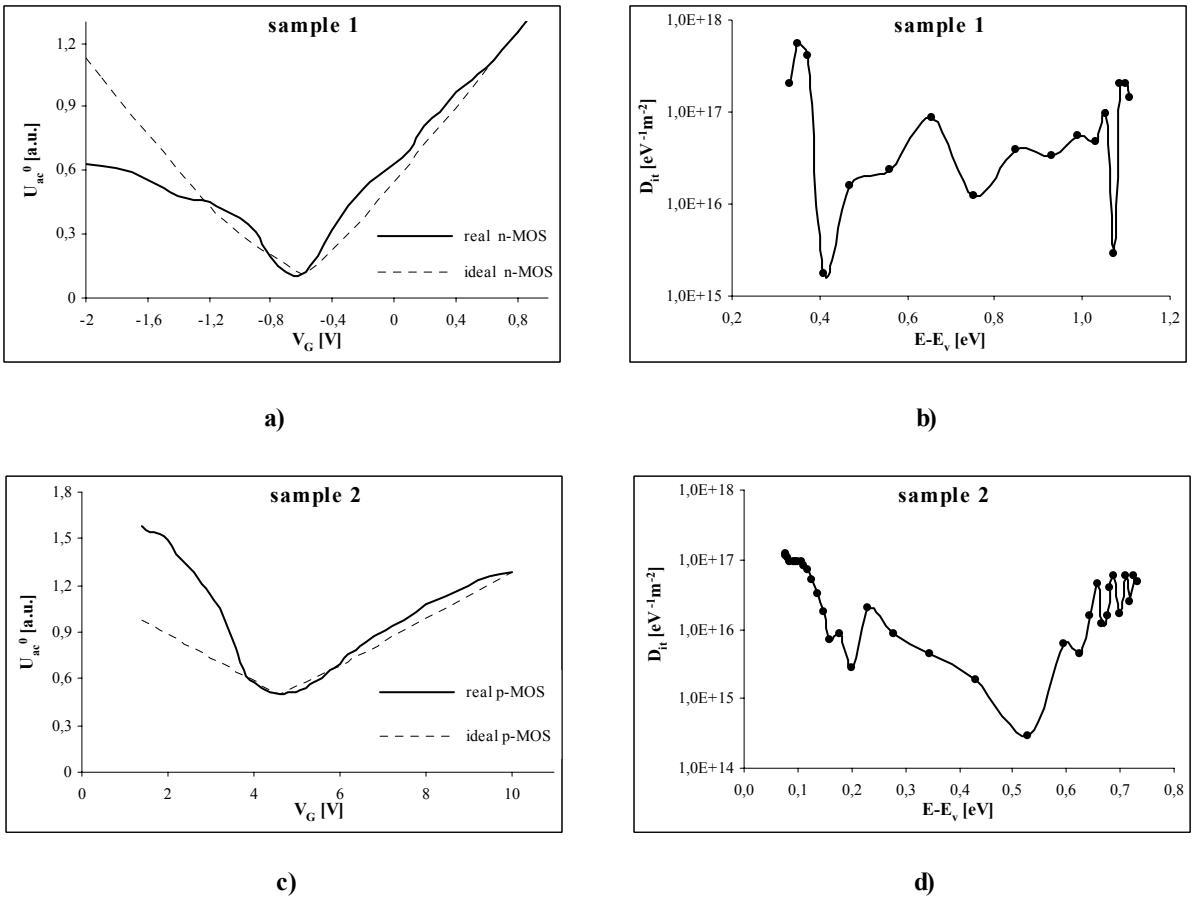

Fig.2: a, c)*The measured and ideal voltage dependence of AER of the Sample 1 resp. 2,* b, d) *The energy distribution of the interface traps in the Sample 1 resp. 2.*

The measured and ideal curves of the AER dependence on the gate bias voltage for Sample 1 are illustrated in Fig. 2a. The corresponding energy distribution is illustrated in Fig. 2b. The Sample 2 was investigated in like manner and the corresponding $U_{ac}^{0}(V_G)$ dependences are illustrated in Fig.2c and calculated density of states in Fig.2d respectively.

5. Conclusion

We indicated that the determination of the interface traps density based on the measurement of the AER can be another useful technique characterizing the interface trap density distribution in MOS structures. However, both additional measurements of different MOS structures and the theoretical improvement of used model should be realised to verify the introduced method properly.

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References:

[1] H. Frank: Physics and technology of semiconductors, SNTL Praha 1990

[2] E. H. Nicollian, J. R. Brews: MOS (Metal Oxide Semiconductor) Physics and Technology, Wiley, New York, 1982.

[3] P. Mason, J. L. Autran, M. Houssa, X. Garros, and C. Lerroux, Appl. Phys. Lett. 81 (2002) 3392

[4] N. Inoue, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, Jap. J. Appl. Phys., 46 (2007) 6480

[5] P. Bury, I. Jamnický, J. Ďurček, Phys. Stat. Sol. (a) 126 (1991) 151

[6] P. Bury, I. Jamnický, Acta Phys. Slovaca 46 (1996) 693

[7] S. J. Song, H. T. Kim, S. S. Chi, M. S. Kim, W. S. Chang, S. D. Cho, H. T. Shin, T. E. Kim, H. J. Kang, D. J. Kim, and D. M. Kim, J. Korean Phys. Soc., 41 (2002) 892